EXHIBIT D

US005841731A

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Shinozaki

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[45] **Date of Patent: Nov. 24, 1998**

[54] **SEMICONDUCTOR DEVICE HAVING EXTERNALLY SETTABLE OPERATION MODE**

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[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **862,298**

[22] Filed: **May 22, 1997**

[30] **Foreign Application Priority Data**

Dec. 13, 1996 [JP] Japan 8-334273

[51] **Int. Cl.**[6] **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/191; 365/201; 365/230.08

[58] **Field of Search** 365/233, 191, 365/201, 230.08

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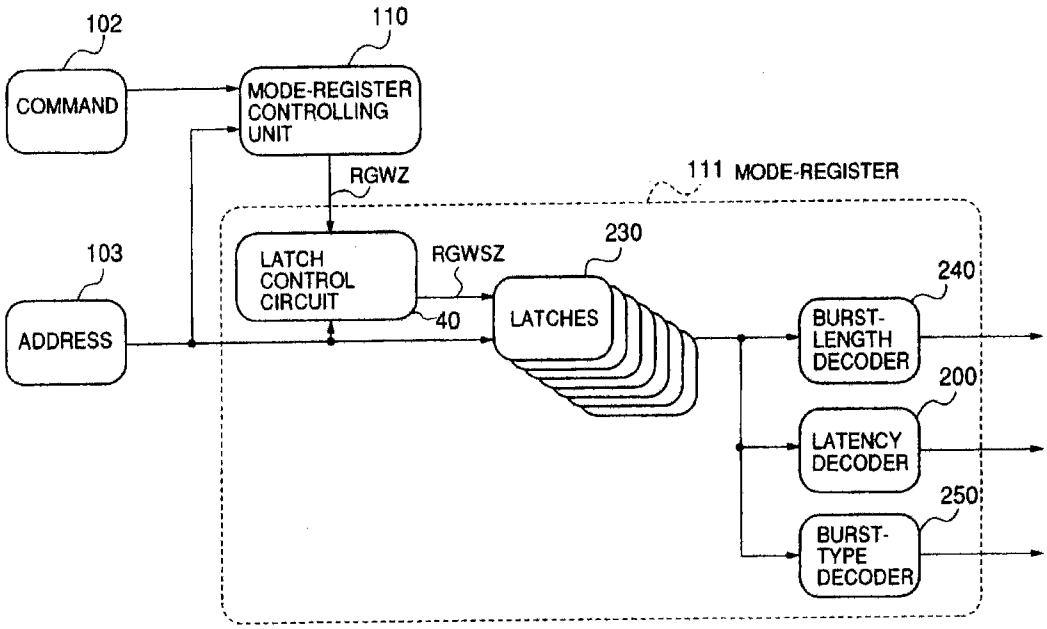
Primary Examiner—David C. Nelms
Assistant Examiner—Hien Nguyen
Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram LLP

[57] **ABSTRACT**

A semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in the one of N operation modes includes a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. The semiconductor device further includes an internal circuit operating in an operation mode selected by the selection circuit.

11 Claims, 8 Drawing Sheets



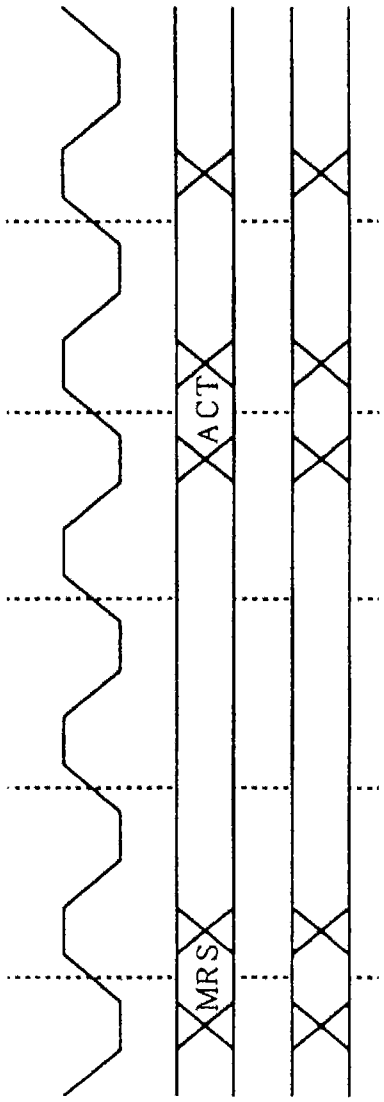


FIG. 1A

FIG. 1B

FIG. 1C

FIG. 1D

FIG. 2

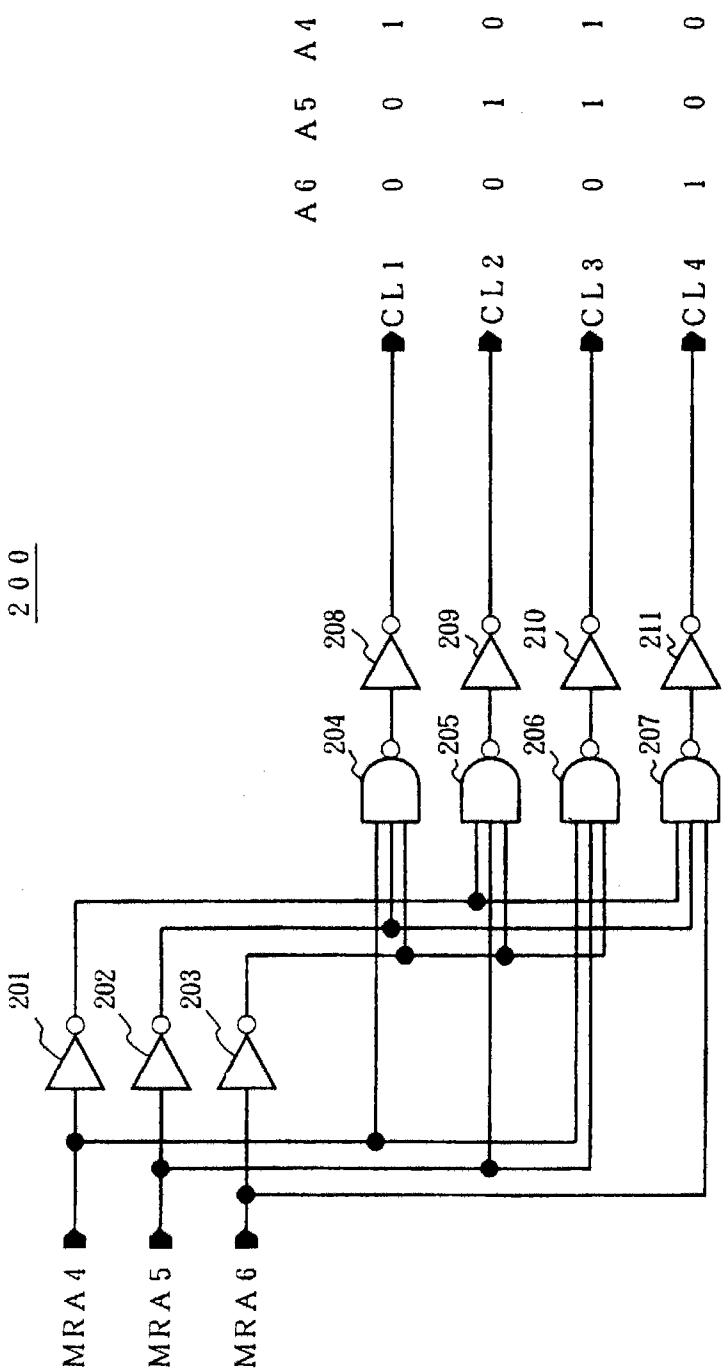

200
A6 A5 A4
0 0 1
0 1 0
0 1 1
1 0 0
CL1
CL2
CL3
CL4
208
209
210
211
204
205
206
207
201
202
203
MRA4
MRA5
MRA6

FIG. 3

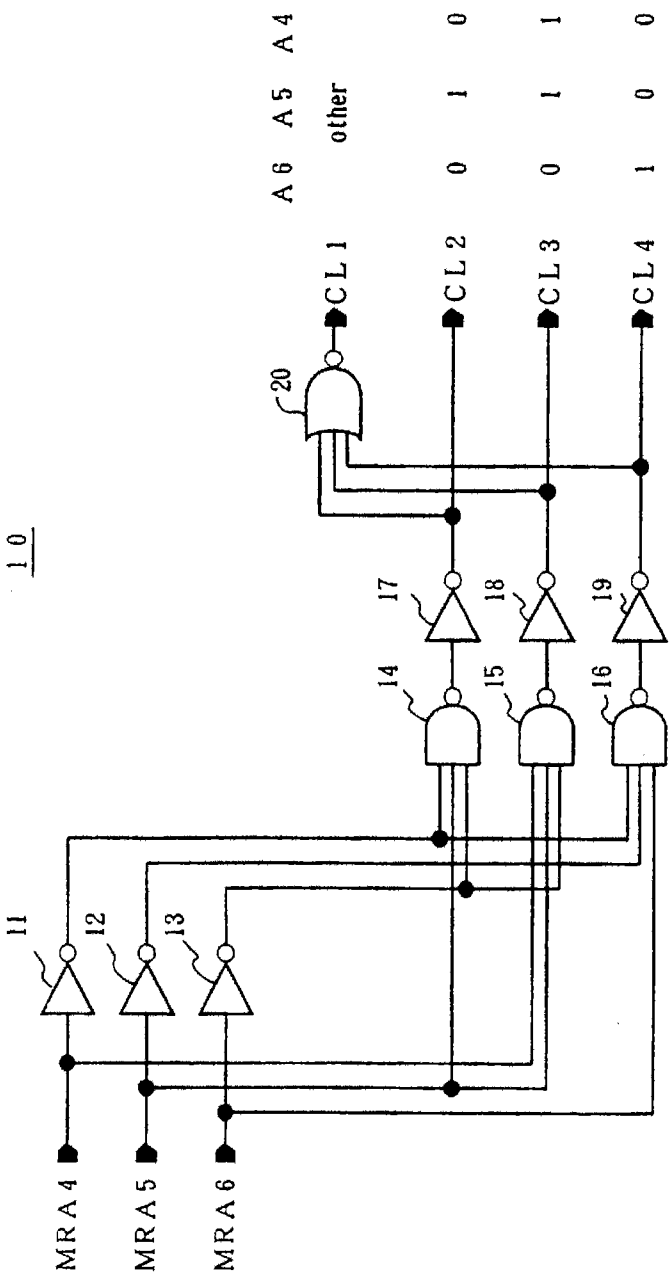

10
A6 A5 A4
other
0 1 0
0 1 1
1 0 0
CL1
CL2
CL3
CL4
20
17
18
19
14
15
16
11
12
13
MRA4
MRA5
MRA6

FIG. 4

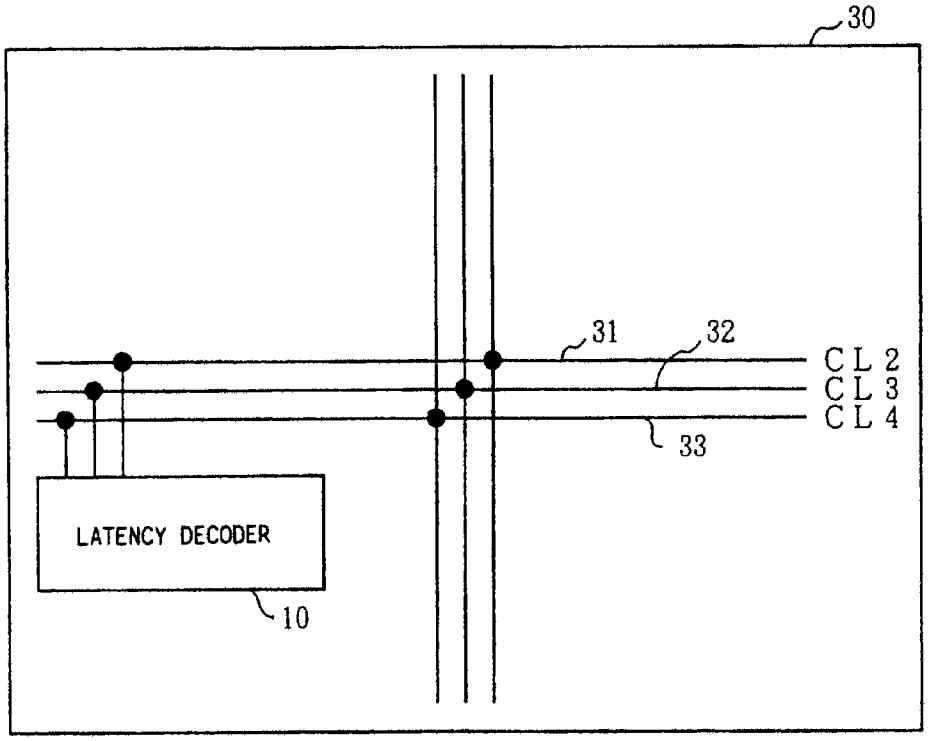


FIG. 6

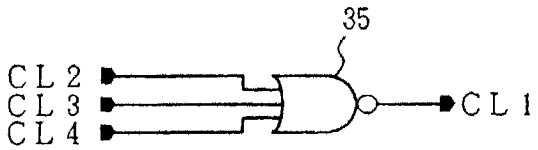


FIG. 5

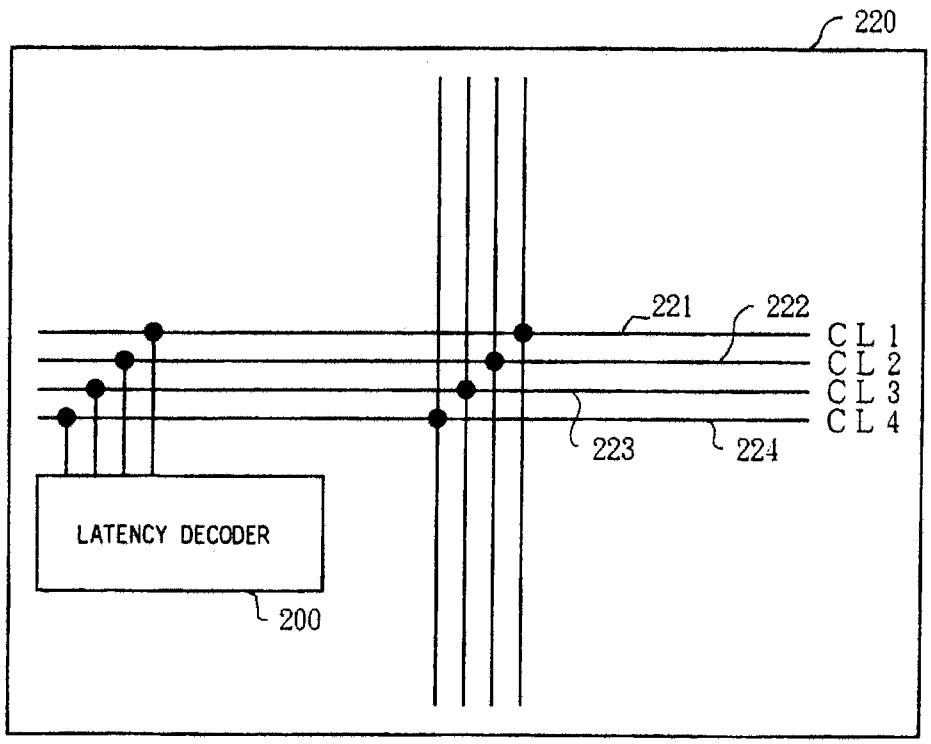


FIG.7

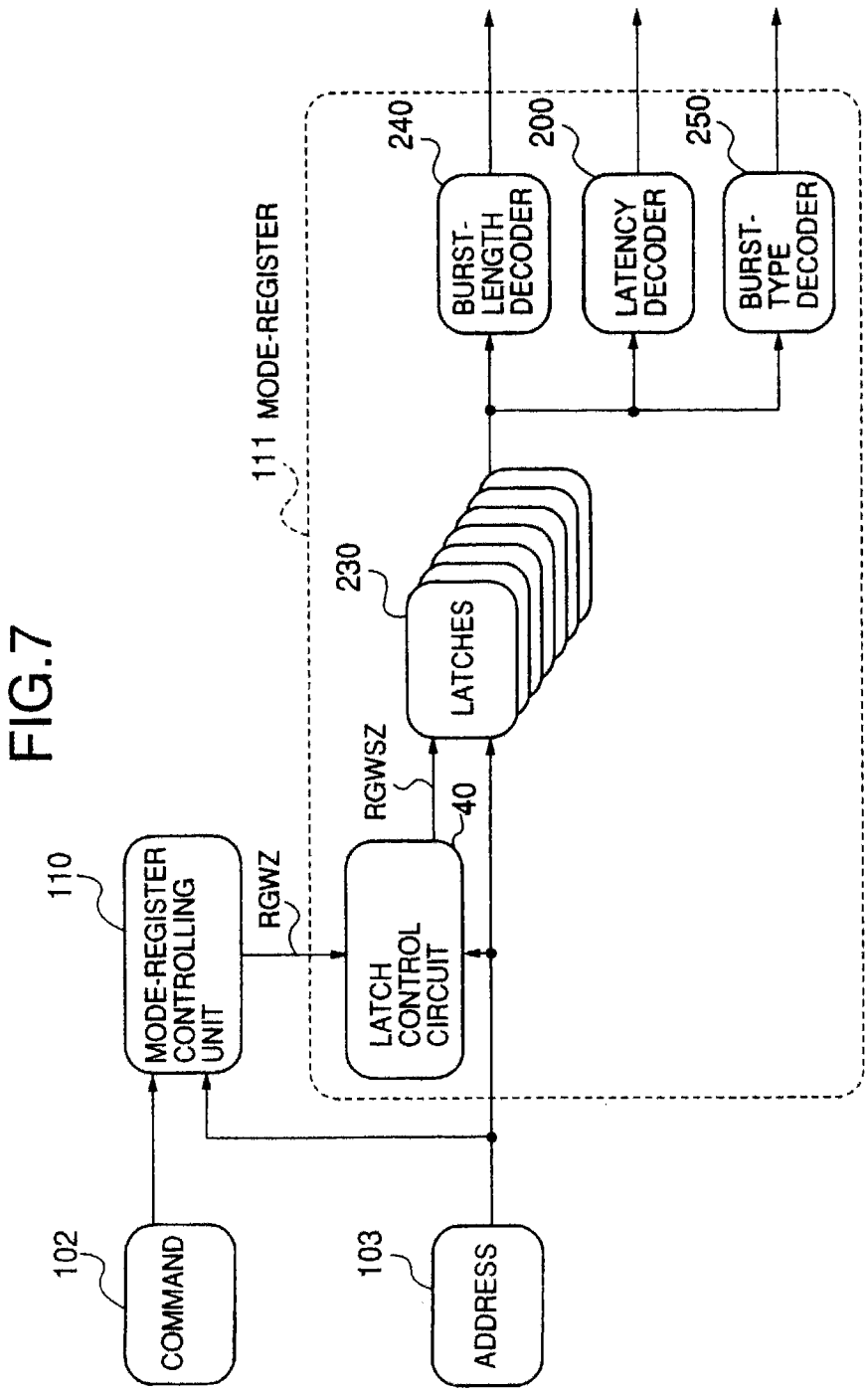

111 MODE-REGISTER
240
BURST-LENGTH DECODER
200
LATENCY DECODER
250
BURST-TYPE DECODER
230
LATCHES
RGWSZ
40
110
MODE-REGISTER CONTROLLING UNIT
RGWZ
LATCH CONTROL CIRCUIT
102
COMMAND
103
ADDRESS

FIG. 8

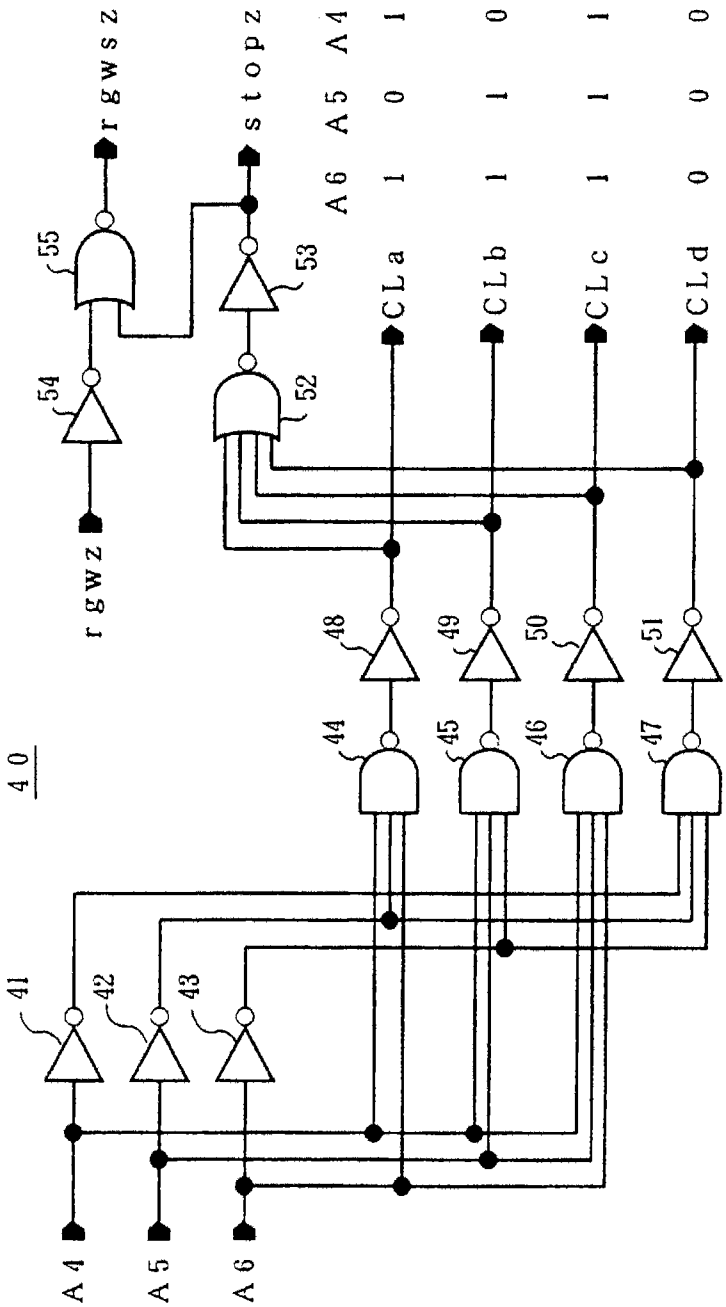
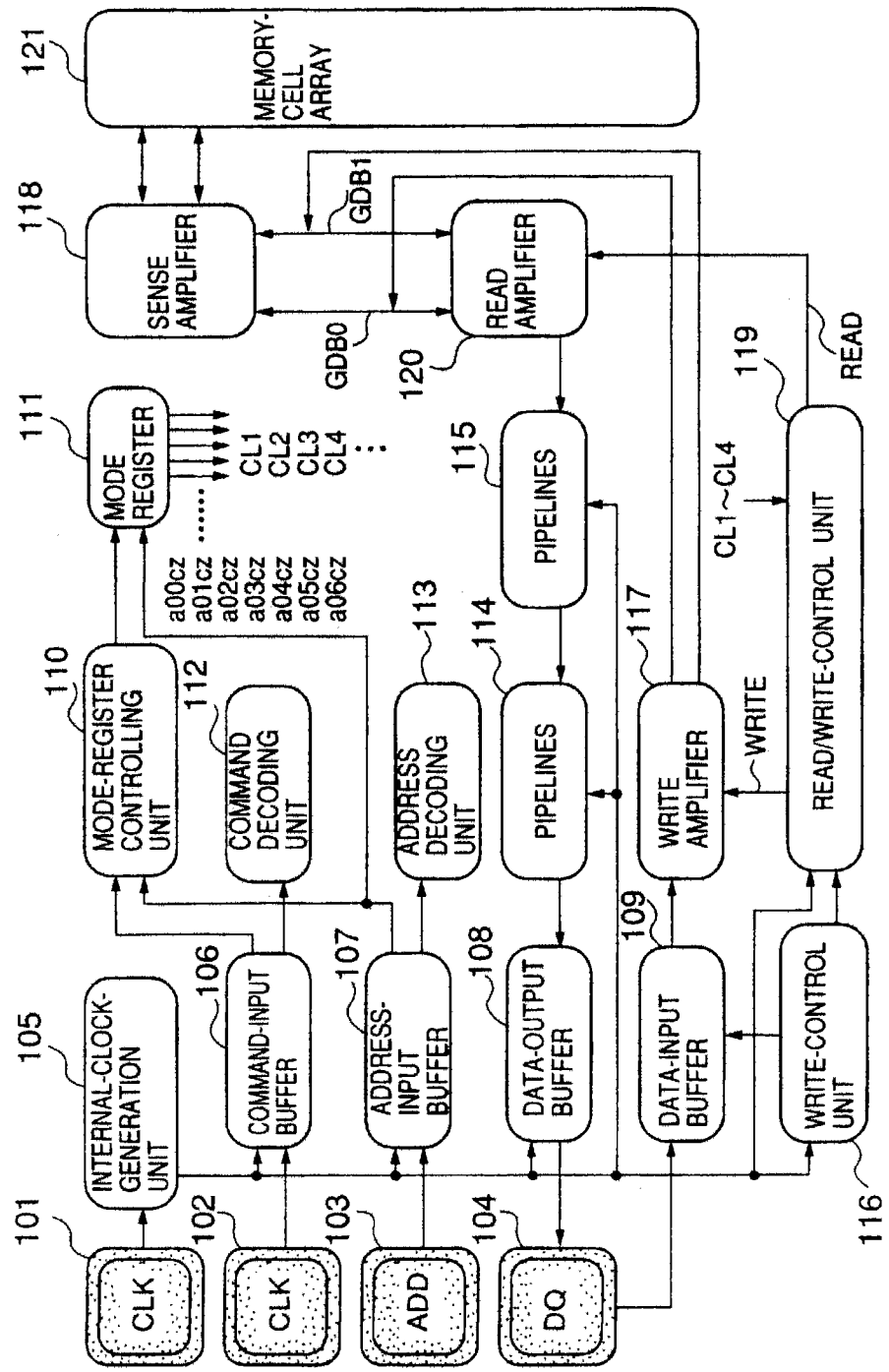

40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
A4
A5
A6
rgwz
rgwsz
stopz
A6 A5 A4
CLa 1 0 1
CLb 1 1 0
CLc 1 1 1
CLd 0 0 0

FIG.9


121
MEMORY-CELL ARRAY
118
SENSE AMPLIFIER
GDB1
GDB0
120
READ AMPLIFIER
119
READ
111
MODE REGISTER
CL1
CL2
CL3
CL4
a00cz
a01cz
a02cz
a03cz
a04cz
a05cz
a06cz
115
PIPELINES
CL1~CL4
110
MODE-REGISTER CONTROLLING UNIT
112
COMMAND DECODING UNIT
113
ADDRESS DECODING UNIT
114
PIPELINES
117
WRITE AMPLIFIER
WRITE
READ/WRITE-CONTROL UNIT
105
INTERNAL-CLOCK-GENERATION UNIT
106
COMMAND-INPUT BUFFER
107
ADDRESS-INPUT BUFFER
108
DATA-OUTPUT BUFFER
109
DATA-INPUT BUFFER
WRITE-CONTROL UNIT
116
101
CLK
102
CLK
103
ADD
104
DQ

SEMICONDUCTOR DEVICE HAVING EXTERNALLY SETTABLE OPERATION MODE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to semiconductor devices, and particularly relates to a semiconductor device which allows an operation mode thereof to be set via an external input.

2. Description of the Related Art

Many types of semiconductor devices are provided with a function to set an operation mode red thereof. In such semiconductor devices, parameters for setting an operation mode are typically stored in a particular register (hereinafter referred to as a mode register).

Conventional SDRAMs, for example, allow parameters for defining an operation mode of the SDRAMs to be set externally, such parameters including a CAS latency, a burst length, a burst type, etc. In setting these parameters, a mode setting operation is instructed via a command input to an SDRAM, and the parameters are input via an address input so as to write these parameters in a mode register of the SDRAM.

FIGS. **1A** through **1D** are illustrative drawings for explaining a mode-register-set operation with respect to a conventional 16M SDRAM. FIG. **1A** shows a clock signal supplied to an SDRAM. FIGS. **1B** and **1C** show a command input and an address input, respectively. As shown in FIGS. **1B** and **1C**, a mode-register-set command MRS is input via the command input, and data is supplied to the address input to store the data in the mode register. After inputting the data, an activation command ACT is fed via the command input to put the newly set mode into effect.

FIG. **1D** shows relations between the data stored in the mode register and the address input. As shown in FIG. **1D**, three bits **A0** through **A2** of the address input together define the burst length, and a bit **A3** represents the burst type. Further, three bits **A4** through **A6** of the address input are used for setting the CAS latency. Bits **A7** through **All** are currently not in use.

Among the parameters, the CAS latency, for example, is a parameter for defining how long a start of a data-read operation is delayed in response to an input of a data-read command. The setting of the CAS latency is made by using the three bits **A4** through **A6** of the address input as described above. This means that eight different types of the setting can be made in principle. Settings currently in use, however, include only three or four different types, so that bit patterns of the three bits **A4** through **A6** include unused patterns.

FIG. **2** is a circuit diagram of a conventional latency decoder. A latency decoder is a circuit included in a mode register. The latency decoder receives three relevant bits from latches also included in the mode register for holding the address-input bits, and decodes these three bits.

A latency decoder **200** of FIG. **2** includes inverters **201** through **203**, NAND circuits **204** through **207**, and inverters **208** through **211**. The inverters **201** through **203** receive data bits MRA**4** through MRA**6**, respectively, which are the address-input bits **A4** through **A6** held by latches. Each of the NAND circuits **204** through **207** receives an non-inverted bit or an inverted bit with respect to each of the data bits MRA**4** through MRA**6**. The inverters **208** through **211** receive outputs of the NAND circuits **204** through **207**, respectively, and invert these outputs.

The outputs of the inverters **208** through **211** are denoted as decode signals CL**1** through CL**4**, respectively, which correspond to respective bit patterns of the address-input bits **A4** through **A6** shown alongside in the figure. Namely, the decode signal CL**1** of the inverter **208**, for example, is a signal which becomes HIGH (selection) when the bits **A4** through **A6** are "100". In the example of FIG. **2**, the latency decoder **200** has four outputs, i.e., the decode signals CL**1** through CL**4**. When the address-input bits **A4** through **A6** have different bit patterns from those shown in the figure, all the decode signals CL**1** through CL**4** become LOW (unselected).

In this manner, all the outputs of the latency decoder **200** end up being unselected when an undefined bit pattern is input. This is not a unique outcome only for the latency decoder **200**, and the same applies in other decoders in the mode register such as a burst-length decoder and a burst-type decoder.

When the CAS latency, the burst length, the burst type, etc., are set in the mode register, entry of an undefined bit pattern which is currently not in use results in all the decoder outputs from the mode register ending up being unselected. When such an undefined setting is made in a conventional semiconductor device such as an SDRAM, it is possible that the chip carries out an unexpected operation which is not cited in a catalog. Such an operation may damage some data stored in memory cells in the case of memory chips.

Accordingly, there is a need for a semiconductor device which insures a normal operation thereof even when an undefined setting is made to a mode register for setting an operation mode of the device.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a semiconductor device which satisfies the need described above.

It is another and more specific object of the present invention to provide a semiconductor device which insures a normal operation thereof even when an undefined setting is made to a mode register for setting an operation mode of the device.

In order to achieve the above objects according to the present invention, a semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in the one of the N operation modes, includes a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. The semiconductor device further includes an internal circuit operating in an operation mode selected by the selection circuit.

In the semiconductor device described above, when an undefined signal is input, one of the N operation modes is selected to prevent an undefined setting from causing an unexpected operation of the semiconductor device.

According to an embodiment of the present invention, the selection circuit includes a first circuit for selecting one of predetermined N−1 operation modes among the N operation modes based on the input signal, while a remaining operation mode is selected when this first circuit does not select any one of the N−1 operation modes. In this configuration, an undefined input leads to a selection of the remaining operation mode, thereby preventing an undefined setting from causing an unexpected operation of the semiconductor device.

According to an embodiment of the present invention, a second circuit for selecting the remaining operation mode based on an output from the first operation mode is provided in proximity of or within the internal circuit. This configuration reduces the number of signal lines from N lines to N−1 lines with respect to the signal transfer of a selected operation mode from the first circuit to the internal circuit.

According to an embodiment of the present invention, the selection circuit includes a circuit for storing the input signal, and a currently stored input signal in this circuit is not updated when an undefined input is given, thereby preventing an undefined setting from causing an unexpected operation of the semiconductor device.

The same objects are also achieved by an equivalent method of selecting one of a plurality of operation modes in a semiconductor device.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** through **1D** are illustrative drawings for explaining a mode-register-set operation with respect to a conventional 16M SDRAM;

FIG. **2** is a circuit diagram of a conventional latency decoder;

FIG. **3** is a circuit diagram of a latency decoder of an SDRAM according to a first embodiment of the present invention;

FIG. **4** is an illustrative drawing showing a layout of signal lines of latency-decode signals inside a semiconductor chip when the latency decoder of FIG. **3** is used;

FIG. **5** is an illustrative drawing showing a conventional layout of signal lines of latency-decode signals inside a semiconductor chip when the latency decoder of FIG. **2** is used;

FIG. **6** is a circuit diagram of an example of a circuit which creates a decode signal CL1 by using decode signals CL2 through CL4;

FIG. **7** is a block diagram showing a mode resister and relating elements in an SDRAM according to a second embodiment of the present invention;

FIG. **8** is a circuit diagram of the latch control circuit of FIG. **7**; and

FIG. **9** is a block diagram of an SDRAM to which the mode register according to the second embodiment of the present invention is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, principles of the present invention will be described with reference to the accompanying drawings.

FIG. **3** is a circuit diagram of a latency decoder of an SDRAM according to a first embodiment of the present invention. The present invention is not limited to use in a latency decoder, but can be applied to other decoders for decoding setting data with regard to a mode register for setting an operation mode of a semiconductor device.

A latency decoder **10** of FIG. **3** includes inverters **11** through **13**, NAND circuits **14** through **16**, inverters **17** through **19**, and a NOR circuit **20**. The inverters **11** through **13** receive data bits MRA4 through MRA6, respectively, which are the address-input bits A4 through A6 held by latches of the mode resister. Each of the NAND circuits **14** through **16** receives a non-inverted bit or an inverted bit with respect to each of the data bits MRA4 through MRA6. The inverters **17** through **19** receive outputs of the NAND circuits **14** through **16**, respectively, and invert these outputs.

The NOR circuit **20** receives the outputs of the inverters **17** through **19**, and outputs a HIGH (selection) signal only when all the outputs of the inverters **17** through **19** are LOW (unselected). The output of the NOR circuit **20** constitutes the decode signal CL1, and the outputs of the inverters **17** through **19** are the decode signals CL2 through CL4, respectively. Conditions which make the decode signals CL1 through CL4 HIGH (selected) are shown by bit patterns of the address-input bits A4 through A6 alongside the decode signals CL1 through CL4 in the figure.

Compared to the latency decoder **200** of FIG. **2**, the latency decoder **10** of FIG. **3** according to the first embodiment has a different condition in which the decode signal CL1 is selected, i.e., the decode signal CL1 becomes HIGH when the decode signals CL2 through CL3 are not selected. Namely, the decode signal CL1 is selected when the address-input bits A4 through A6 are "100" as in the latency decoder **200** of FIG. **2**, and, also, is selected when an undefined setting is made.

Accordingly, the use of a decoder having the configuration as shown in FIG. **3** makes it possible to avoid malfunction of a semiconductor device even when an undefined setting is made. This is achieved by allocating undefined settings to one of the defined outputs.

FIG. **4** is an illustrative drawing showing a layout of signal lines of latency-decode signals inside a semiconductor chip when the latency decoder **10** of FIG. **3** is used. FIG. **5** is an illustrative drawing showing a conventional layout of signal lines of latency-decode signals inside a semiconductor chip when the latency decoder **200** of FIG. **2** is used.

In the layout shown in FIG. **5**, long-distance lines **221** through **224** are provided to transfer the decode signals CL1 through CL4 from the latency decoder **200** of FIG. **2** to other units inside a chip **220**. On the other hand, the layout of FIG. **4** includes long-distance lines **31** through **33** to transfer only the decode signals CL2 through CL4 inside a chip **30** from the latency decoder **10** of FIG. **3**. Since the decode signal CL1 is selected only when the decode signals CL2 through CL4 are unselected, there is no need to transfer the decode signal CL1 to other units via a long-distance line.

In each of the units using the latency-decode signals, the decode signal CL1 can be created based on the decode signals CL2 through CL4 sent from the latency decoder **10**.

FIG. **6** is a circuit diagram of an example of a circuit which creates the decode signal CL1 by using the decode signals CL2 through CL4. A NOR circuit **35** of FIG. **6** receives the decode signals CL2 through CL4, and outputs a HIGH (selection) signal only when all the received signals are LOW (unselected). Namely, the output of the NOR circuit **35** is the same as the decode signal CL1.

The circuit as shown in FIG. **6** can be provided for each unit which uses the latency decode signals, thereby eliminating a need to transfer the decode signal CL1 via a long-distance line. Since a long-distance line occupies a larger space than a simple circuit such as shown in FIG. **6**, efficient use of space inside a chip is achieved by eliminating one of the long-distance lines by providing the circuit of FIG. **6** for each unit.

The NOR circuit **35** of FIG. **6** can be regarded as the NOR circuit **20** of FIG. **3** which is relocated from inside the mode register to each unit which requires the decode signals. Namely, when a layout as shown in FIG. **4** is used, the NOR

circuit **20** of FIG. **3** is removed, and the NOR circuit **35** of FIG. **6** is provided for each unit as a substitute for the removed NOR circuit **20**.

FIG. **7** is a block diagram showing a mode register and relating elements in an SDRAM according to a second embodiment of the present invention. FIG. **7** shows a command-signal-input node **102**, an address-signal-input node **103**, a mode-register controlling unit **110**, and a mode register **111**. The mode register **111** includes a latch control circuit **40**, latches **230**, a burst-length decoder **240**, the latency decoder **200** of FIG. **2**, and a burst-type decoder **250**. The configuration of FIG. **7** is the same as that of a conventional mode register and relating elements, except that the latch control circuit **40** is newly provided.

A command signal (see FIG. 1B) input to the command-signal-input node **102** is supplied to the mode-register controlling unit **110**. An address signal (see FIG. 1C) input to the address-signal-input node **103** is provided to the mode-register controlling unit **110** and the mode register **111**. The mode-register controlling unit **110** outputs an enable signal rgwz in accordance with timing of the address signal when the received command signal instructs to set the mode register. In a conventional configuration, the enable signal rgwz received by the mode register **111** is directly supplied to the latches **230**, and the latches **230** latch the address signal.

In the second embodiment of the present invention, the enable signal RGWZ received by the mode register **111** is first supplied to the latch control circuit **40**. The latch control circuit **40** receives the address signal in addition to the enable signal rgwz, and determines based on the contents of the address signal whether to provide the enable signal rgwz to the latches **230**. In detail, the latch control circuit **40** does not supply the enable signal rgwz to the latches **230** when the address signal shows a bit pattern of an undefined setting.

FIG. **8** is a circuit diagram of the latch control circuit **40**. The latch control circuit **40** of FIG. **8** includes inverters **41** through **43**, NAND circuits **44** through **47**, inverters **48** through **51**, a NOR circuit **52**, inverters **53** and **54**, and a NOR circuit **55**. The inverters **41** through **43** receive the bits **A4** through **A6** of the address signal, respectively. Each of the NAND circuits **44** through **47** receives a non-inverted bit or an inverted bit with respect to each of the address-input bits **A4** through **A6**. The inverters **48** through **51** receive outputs of the NAND circuits **44** through **47**, respectively, and invert these outputs.

The outputs of the inverters **48** through **51** are decode signals CLa through CLd. Conditions in which these decode signals CLa through CLd are selected to turn into HIGH are shown in FIG. **8** as bit patterns of the address-input bits **A4** through **A6**. As can be seen from a comparison with the bit patterns of the address-input bits **A4** through **A6** shown in FIG. **2**, the bit patterns for the decode signals CLa through CLd of FIG. **8** correspond to undefined bit patterns. Namely, the inverters **48** through **51** of FIG. **8** produce outputs, one of which is HIGH when an undefined bit pattern is entered.

The NOR circuit **52** receives decode signals CLa through CLd. The NOR circuit **52** outputs a LOW signal when one of the decode signals CLa through CLd is HIGH, and outputs a HIGH signal when all the decode signals CLa through CLd are LOW. The inverter **53** inverts the output of the NOR circuit **52**. An output of the inverter **53** is shown as a control signal stopz. The control signal stopz becomes HIGH when one of the decode signals CLa through CLd is HIGH, i.e., when an undefined input is made.

The control signal stopz is supplied to one input of the two-input NOR circuit **55**. The other input of the NOR circuit **55** receives the inverse of the enable signal rgwz obtained by the inverter **54**.

When the control signal stopz is HIGH, the output of the NOR circuit **55** is LOW at all the times. The enable signal rgwz is thus blocked by the NOR circuit **55**. When the control signal stopz is LOW, the NOR circuit **55** serves as an inverter for the inverse of the enable signal rgwz. The NOR circuit **55** thus outputs the enable signal rgwz by inverting the inverse of the enable signal rgwz.

The output of the NOR circuit **55** is supplied to the latches **230** as a latch-control signal rgwsz (see FIG. **7**). In this manner, the latch control circuit **40** blocks the enable signal rgwz when an undefined input is made, and outputs the enable signal rgwz as the latch-control signal rgwsz when a defined input is made. Having received the latch-control signal rgwsz, the latches **230** latch the address-input bits **A0** through **A06**.

As described above, the mode register **111** according to the second embodiment of the present invention shown in FIG. **7** and FIG. **8** can avoid malfunction of an SDRAM when an undefined input is attempted because no setting is made to the CAS latency when an undefined input is made.

In the configuration shown in FIG. **7** and FIG. **8**, when an undefined input is made with respect to a burst length, the undefined input is held by the latches **230**, and is decoded by the burst-length decoder **240** to be output. (There is no undefined setting for a burst type since the burst type is represented by only one bit.) If one wishes to provide an anti-malfunction mechanism also for the burst length, therefore, one may modify the circuit of FIG. **8** so as to detect an undefined input with respect to the bits **A0** through **A2**.

The second embodiment of the present invention has a configuration such that when an undefined input is made, data writing to the mode register is prohibited by detecting the undefined input. It is apparent that this configuration is not limited to application only to a mode register of SDRAMs, but can be applied to various semiconductor devices.

FIG. **9** is a block diagram of an SDRAM to which the mode register according to the second embodiment of the present invention is applied. The SDRAM of FIG. **9** includes a clock-signal-input node **101**, the command-signal-input node **102**, the address-signal-input node **103**, a data-signal-input/output node **104**, an internal-clock-generation unit **105**, a command-input buffer **106**, an address-input buffer **107**, a data-output buffer **108**, a data-input buffer **109**, the mode-register controlling unit **110**, the mode register **111** shown in FIG. **7**, a command decoding unit **112**, an address decoding unit **113**, pipelines **114** and **115**, a write-control unit **116**, a write amplifier **117**, a sense amplifier **118**, a read/write-control unit **119**, a read amplifier **120**, and a memory-cell array **121**.

The SDRAM of FIG. **9** has the same configuration as that of a conventional SDRAM, except that the mode register **111** of the present invention is used.

In the following, operations of the SDRAM of FIG. **9** will be described in brief. A clock signal input to the clock-signal-input node **101** is supplied to the internal-clock-generation unit **105**, which generates various internal clock signals for controlling the internal circuits. Based on internal clock signals generated by the internal-clock-generation unit **105**, the command-input buffer **106**, the address-input buffer **107**, and the data-input buffer **109** read a command signal,

an address signal, and a data signal from the command-signal-input node **102**, the address-signal-input node **103**, and the data-signal-input/output node **104**, respectively.

The command signal is supplied from the command-input buffer **106** to the command decoding unit **112** to be decoded. Based on the decoding results, the internal circuits are controlled. When a mode-register setting command is provided as a command, the mode-register controlling unit **110** writes an address signal from the address-input buffer **107** in the mode register **111** in response to the mode-register setting command.

The address signal is supplied from the address-input buffer **107** to the address decoding unit **113** for decoding. Based on the address decoding results, the memory-cell array **121** is accessed at an indicated address thereof.

The data signal is stored in the memory-cell array **121** at the indicated address thereof, supplied from the data-input buffer **109** via the write amplifier **117** and the sense amplifier **118**. On the other hand, data read from the memory-cell array **121** at the indicated address thereof is supplied to the data-output buffer **108** via the sense amplifier **118**, the read amplifier **120**, and the pipelines **114** and **115**. The data-output buffer **108** outputs the data to the data-signal-input/output node **104** based on an internal clock generated by the internal-clock-generation unit **105**.

The write-control unit **116** supplies a control signal to the read/write-control unit **119** in accordance with the command decoding results of the command decoding unit **112**. Also, based on the command decoding results, the write-control unit **116** controls the data-input buffer **109**.

The read/write-control unit **119** generates control signals such as a write signal Write, a read signal Read, a column-line selecting signal (not shown), etc. The column-line selecting signal, for example, is supplied to the sense amplifier **118** which is comprised of a plurality of sense amplifiers, and allows data to be written in or read from selected sense amplifiers for a predetermined time period. The write signal Write is supplied to the write amplifier **117** so as to provide the input data from the data-input buffer **109** to global data bus GDB**0** and GDB**1** at a predetermined timing. The read signal Read is supplied to the read amplifier **120** so as to provide the read data from the global data bus GDB**0** and GDB**1** to the pipeline **115** at a predetermined timing.

The mode register **111** stores settings of the burst length, the burst type, the CAS latency, etc., as previously described. As for the CAS latency, for example, the mode register **111** outputs the CAS-latency indicating signals (decode signals) CL**1** through CL**4** for indicating which CAS latency is being used. (When the number of CAS latencies which can be set is more than **4**, a CAS-latency indicating signal CL**5** and so on are also generated.) Based on the CAS-latency indicating signals CL**1** through CL**4**, the read/write-control unit **119** controls the timing of a data-read operation.

As described in connection with FIG. **7** and FIG. **8**, when an attempt is made to set an undefined CAS latency in the mode register **111**, this undefined CAS latency is prevented from being written in the mode register **111**. In the SDRAM of FIG. **9**, therefore, a malfunction can be avoided even when an undefined input is attempted for the CAS latency. Further, it is obvious that the function of preventing undefined input can be provided for other parameters such as a parameter for the burst length in addition to the CAS latency.

In the SDRAM of FIG. **9**, the mode register **111** of FIG. **7** may be replaced by a conventional mode register, and the latency decoder of FIG. **3** may be provided in this replacing mode register. In this case, when an undefined setting is attempted for the CAS latency, the CAS-latency indicating signal CL**1**, for example, is selected, thereby avoiding a malfunction of the SDRAM. In this configuration, signal lines inside the SDRAM for transferring the CAS-latency indicating signals may be provided only for the CAS-latency indicating signals CL**2** through CL**4**, and the NOR circuit of FIG. **6** may be provided in relevant circuit units such as the read/write-control unit **119**.

Further, the present invention is not limited to these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

What is claimed is:

1. A semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in said one of N operation modes, said semiconductor device comprising:

a selection circuit for selecting an operation mode from said N operation modes when said input signal indicates said operation mode, and for selecting a predetermined operation mode from said N operation modes when said input signal is an undefined signal indicating none of said N operation modes; and

an internal circuit operating in one of said operation mode and said predetermined operation mode selected by said selection circuit,

wherein selection of said predetermined operation mode prevents malfunction of said internal circuit when said input signal is said undefined signal.

2. The semiconductor device as claimed in claim **1**, wherein said selection circuit comprises:

a first circuit for selecting one of predetermined N−1 operation modes among said N operation modes by decoding said input signal; and

a second circuit for selecting, based on logic operation of outputs of said first circuit, a remaining operation mode of said N operation modes when none of said predetermined N−1 operation modes is selected.

3. The semiconductor device as claimed in claim **2**, wherein said selection circuit further comprises N−1 signal lines connecting between said first circuit and said second circuit, and said second circuit is located in a proximity of said internal circuit or within said internal circuit.

4. The semiconductor device as claimed in claim **1**, wherein said selection circuit comprises:

a third circuit for detecting said undefined signal;

a fourth circuit, responsive to an output from said third circuit, for storing said input signal when said input signal is not said undefined signal, and for holding a currently stored input signal when said input signal is said undefined signal; and

a fifth circuit for selecting one of said N operation modes by decoding said input signal stored in said fourth circuit.

5. A semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in said one of N operation modes, said semiconductor device comprising:

a selection circuit for selecting an operation mode from said N operation modes when said input signal indicates said operation mode, and for selecting a predetermined operation mode from said N operation modes when said input signal is an undefined signal indicating none of said N operation modes;

a core circuit for storing data; and

a control circuit operating in one of said operation mode and said predetermined operation mode selected by said selection circuit to control said core circuit,

wherein selection of said predetermined operation mode prevents malfunction of said control circuit when said input signal is said undefined signal.

6. The semiconductor device as claimed in claim **5**, wherein said selection circuit comprises:

a first circuit for selecting one of predetermined N−1 operation modes among said N operation modes by decoding said input signal; and

a second circuit for selecting, based on logic operation of outputs of said first circuit, a remaining operation mode of said N operation modes when none of said predetermined N−1 operation modes is selected.

7. The semiconductor device as claimed in claim **6**, wherein said selection circuit further comprises N−1 signal lines connecting between said first circuit and said second circuit, and said second circuit is located in a proximity of said control circuit or within said control circuit.

8. The semiconductor device as claimed in claim **5**, wherein said selection circuit comprises:

a third circuit for detecting said undefined signal;

a fourth circuit, responsive to an output from said third circuit, for storing said input signal when said input signal is not said undefined signal, and for holding a currently stored input signal when said input signal is said undefined signal; and

a fifth circuit for selecting one of said N operation modes by decoding said input signal stored in said fourth circuit.

9. A method of selecting one of a plurality of operation modes in a semiconductor device by using an input signal, said method comprising the steps of:

selecting an operation mode from said plurality of operation modes when said input signal indicates said operation mode; and

selecting a predetermined operation mode from said plurality of operation modes when said input signal is an undefined signal indicating none of said plurality of operation modes.

10. A method of selecting one of N operation modes in a semiconductor device by using an input signal, said method comprising the steps of:

selecting one of predetermined N−1 operation modes among said N operation modes by decoding said input signal; and

selecting a remaining operation mode of said N operation mode when none of said N−1 operation modes is selected.

11. A method of selecting one of a plurality of operation modes in a semiconductor device by using an input signal, said method comprising the steps of:

detecting whether said input signal is an undefined signal indicating none of said plurality of operation modes;

storing said input signal to a register when said input signal is not an undefined signal;

holding said input signal currently stored in said register when said input signal is an undefined signal; and

selecting one of said plurality of operation modes by decoding said input signal stored in said register.

* * * * *

EXHIBIT E

United States Patent [19]

Takemae

[11] **Patent Number: 4,692,689**

[45] **Date of Patent: Sep. 8, 1987**

[54] **FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION**

[75] Inventor: **Yoshihiro Takemae**, Tokyo, Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **15,529**

[22] Filed: **Feb. 12, 1987**

Related U.S. Application Data

[63] Continuation of Ser. No. 663,712, Oct. 22, 1984, abandoned.

[30] **Foreign Application Priority Data**

Nov. 11, 1983 [JP] Japan 58-212083

[51] **Int. Cl.**[4] **G05F 3/24**

[52] **U.S. Cl.** **323/313**; 307/297; 307/304; 323/314; 323/349; 323/350; 365/226

[58] **Field of Search** ..... 323/311, 313, 349, 350, 323/314; 307/296 R, 297, 304; 365/226

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Primary Examiner—William H. Beha, Jr.

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A voltage converting circuit has an output MIS transistor which gives a low output impedance and outputs an intermediate level of power source voltage. The output level is set with a high accuracy through a voltage dividing ratio determined by an impedance element. This impedance element is connected with a compensating MIS transistor to compensate for variations of the gate threshold voltage caused by the manufacturing process.

10 Claims, 9 Drawing Figures

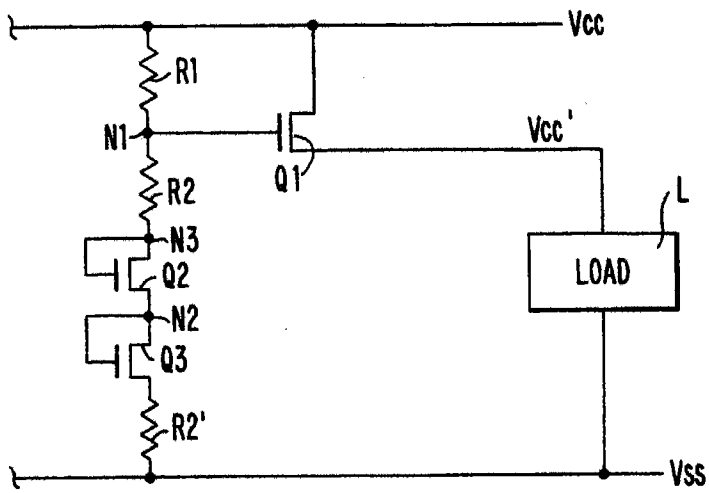


FIG. 1.
(PRIOR ART)

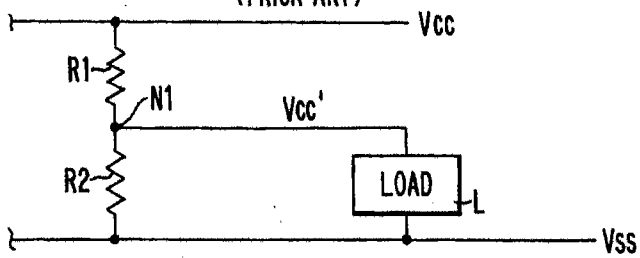


FIG. 2.
(PRIOR ART)

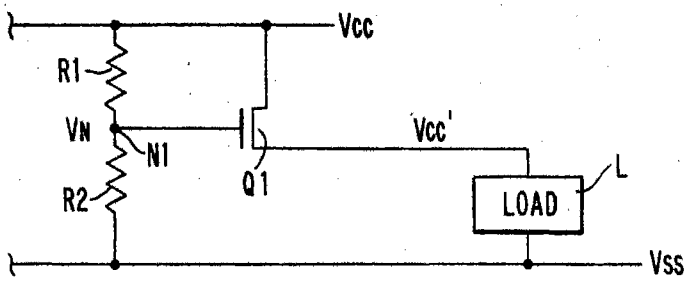


FIG. 8.

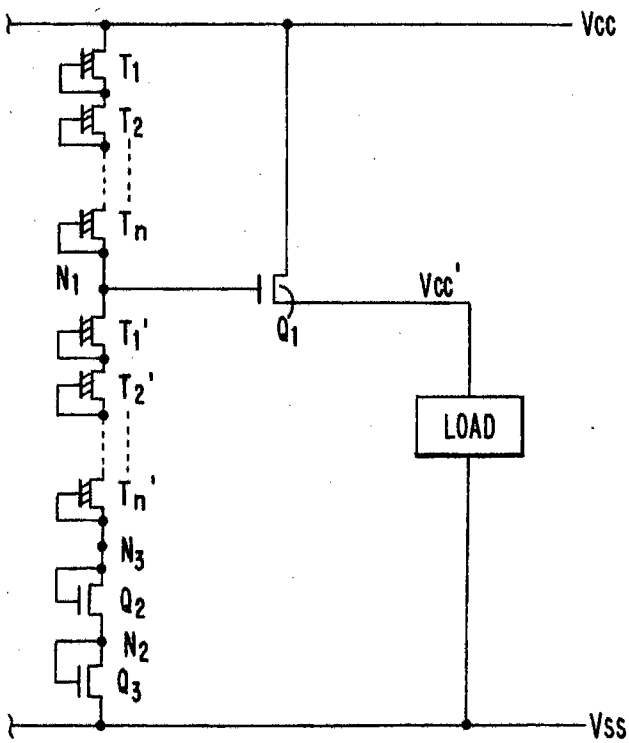


FIG. 3.

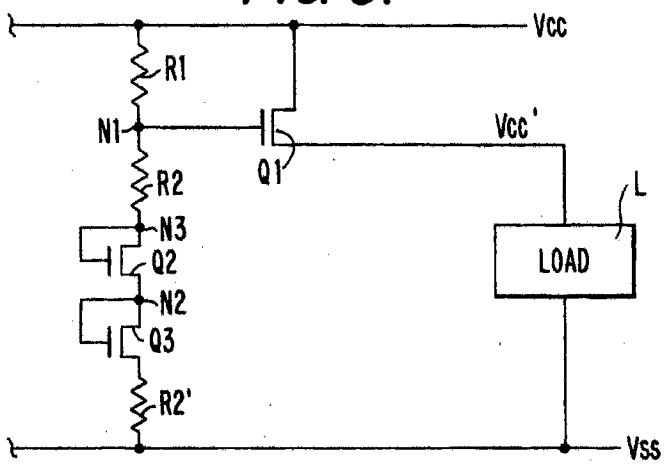


FIG. 4.

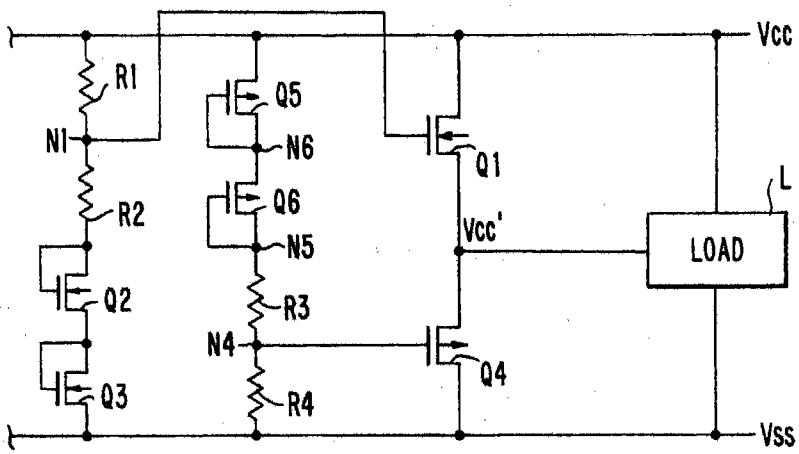


FIG. 5.

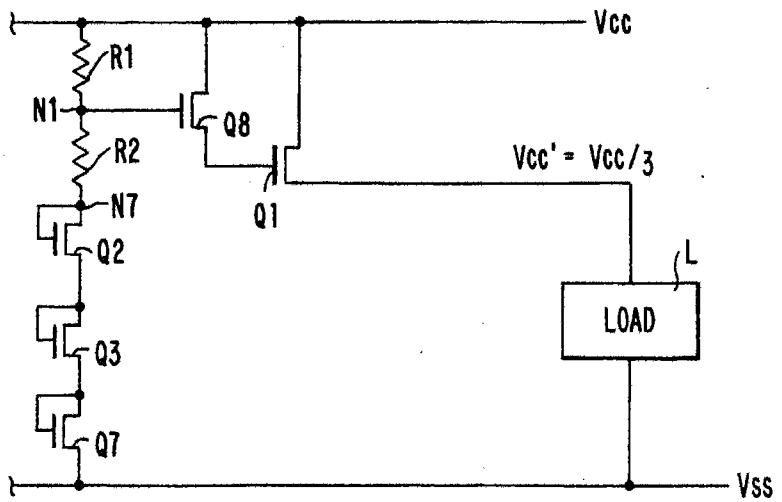


FIG. 6.

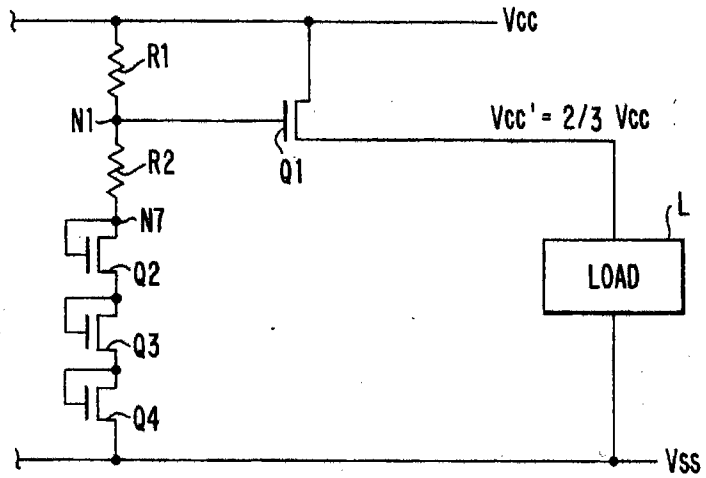


FIG. 7(a)

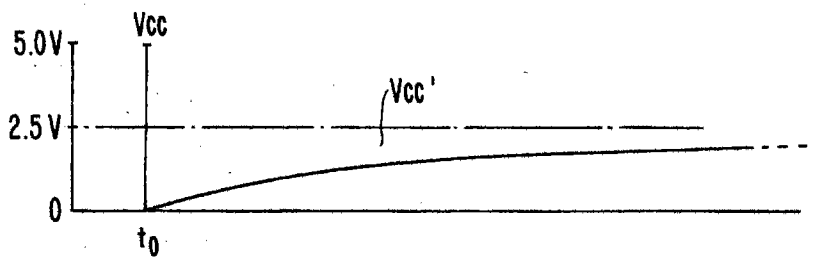
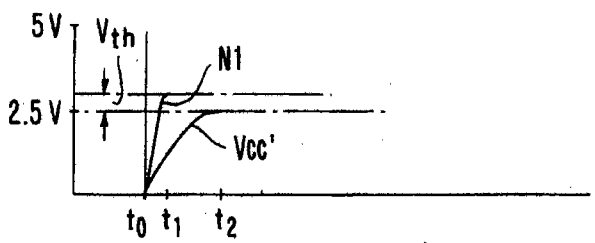


FIG. 7(b)



FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION

This is a continuation of co-pending application Ser. No. 663,712 filed on Oct. 22, 1984, now abandoned 2/12/87.

BACKGROUND OF THE INVENTION

This invention relates to a voltage converting circuit which outputs an intermediate level of power supply voltage and particularly to a voltage converting circuit which is suitable for use in a MIS type integrated circuit.

It is often required in a MIS type integrated circuit to use a constant voltage having an intermediate level with respect to the power supply voltage supplied from an external circuit. For instance, an intermediate level of, for example, 2.5 V is steadily applied to a common capacitor electrode incorporated into memory cells in a MIS type dynamic random access memory operative under a power supply voltage of 5 V.

The intermediate level is obtained easily using a resistance dividing circuit as shown on FIG. 1. In this figure, resistors R_1, R_2 divide the power supply voltage V_{cc} in order to obtain an intermediate voltage V_{cc}' to be provided to a load circuit L. For a sufficiently low load current, when $R_1=R_2$, then $V_{cc}'=V_{cc}/2$. However, when a load circuit L consumes a current that is sufficiently high, such a relation is not maintained. Moreover, in this example, the resistors R_1, R_2 are connected in series between the power source V_{cc} of +5 V and the power source V_{ss} of 0 V, a current always flows from V_{cc} to V_{ss}, and thereby a large amount of power is consumed. This is one disadvantage of this circuit. Such power consumption can be reduced by making large the resistors R_1, R_2. However, if a resistance value is large, the above change in the voltage V_{cc}' at node N1 due to a load current becomes large.

The circuit shown in FIG. 2 is effective for reducing power consumption and fluctuation of the load voltage V_{cc}' due to a change of the load current. In this circuit, a divided voltage of power source V_{cc} obtained through the resistors R_1, R_2 is given to the gate of a MIS transistor Q_1 and an output of said transistor Q_1 is applied to the load circuit L. Q_1 constitutes an output transistor of low output impedance. Therefore, a load current flows through the drain and source of transistor Q_1 but does not flow into the voltage dividing circuit R_1, R_2. There is no change of load voltage V_{cc}' and, since the dividing circuit only gives a voltage to the gate of the MIS transistor Q_1, the circuit is allowed to have a high resistance value, thus resulting in less power consumption. Because of the relation $V_N-V_{th}=V_{cc}'$ between the voltage V_N of node N_1 and load voltage V_{cc}', when $V_{cc}'=V_{cc}/2$ is required, V_N is selected to have a value satisfying the relation, $V_N=V_{th}+V_{cc}/2$. V_{th} indicates the gate threshold voltage of the MIS transistor Q_1.

However, this circuit has a problem in that a threshold voltage V_{th} of the transistor Q_1 directly affects a load voltage V_{cc}' and V_{th} changes in accordance with the integration circuit manufacturing process, whereby the load voltage V_{cc}' fluctuates for each product.

Namely, it is well known that a resistance ratio of two resistors in an integrated circuit has only a small error, although there are changes of V_{th} depending on the manufacturing process. For example, it is easy to ensure that an error of resistance value ratio is as small as 1% or less. Therefore, a voltage V_N of node N_1 can be set accurately. Meanwhile, the gate threshold voltage of a MIS transistor is easily affected by a process fluctuation, and an error as small as 0.2 V can easily be generated. This error means, for example, that an error of about 10% easily occurs in the circuit for generating an output voltage V_{cc}' of 2.5 V.

SUMMARY OF THE INVENTION

An object of this invention is to provide a voltage converting circuit which outputs an intermediate level of power source voltage.

Another object of this invention is to provide a voltage converting circuit which consumes less power.

Yet another object of this invention is to provide a voltage converting circuit comprising an output MIS transistor which gives a small output impedance.

A further object of this invention is to prevent an output voltage from being affected by a variation of the threshold voltage V_{th} caused by a fluctuation in the manufacturing process for output MIS transistors of voltage converting circuits.

In accordance with the present invention, a voltage converting circuit is provided for receiving a power source voltage and providing a constant voltage having the level of a predetermined porportional division of said power source voltage, comprising:

an output MIS transistor for outputting said constant voltage, with the MIS transistor having a gate which receives a gate control voltage; and

a gate control means for providing said gate of said MIS transistor with said gate control voltage, comprising an impedance means connected to receive said power source voltage for providing said predetermined proportional division, and compensating means having at least one compensation MIS transistor connected to said impedance means, for compensating the gate control voltage for the gate threshold voltage of said output MIS transistor to provide said constant voltage corresponding to said predetermined proportional division irrespective of variation of said gate threshold voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the present invention will be more apparent from the following description of the preferred embodiments with reference to the accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a voltage converting circuit in the prior art;

FIG. 2 is a schematic diagram of the other voltage converting circuit in the prior art;

FIG. 3 is a schematic diagram of a voltage converting circuit in an embodiment of this invention;

FIG. 4 is a schematic diagram of a voltage converting circuit in another embodiment of this invention;

FIG. 5 is a schematic diagram of a voltage converting circuit in yet another embodiment of this invention;

FIG. 6 is a schematic diagram of a voltage converting circuit in a further embodiment of this invention;

FIGS. 7(*a*) and (*b*) are respective the graphs which show the change in time of the converted voltage output after the power source is turned ON in the circuits of the prior art and of the embodiments of this invention; and

FIG. 8 is a schematic diagram of a voltage converting circuit in still a further embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 3 shows an embodiment of this invention. From FIG. 1 to FIG. 8, the same portions as those in FIG. 1 and FIG. 2 are given the same symbols for convenience of description. In comparison with the circuit of the prior art as shown in FIG. 2, the circuit of FIG. 3 is different therefrom in such a point that the MIS transistors Q_2, Q_3 are inserted into the voltage dividing circuit (gate voltage control circuit). In the circuit of FIG. 3, a pair of N channel MIS transistors Q_2, Q_3 are connected in series to the resistor elements R_1 and R_2 which give a voltage dividing ratio. A divided output from the series circuit of resistor elements R_1, R_2 and MIS transistors Q_2, Q_3 is given at the node N_1 to the gate of the output N channel MIS transistor Q_1. The transistors Q_2, Q_3 are provided for compensating its gate threshold voltage, and the number of transistors depends on the voltage dividing ratio. The circuit of FIG. 3 is provided for outputting a voltage of $V_{cc}/2$ and two transistors Q_2 and Q_3 are required in this case. Said circuit of FIG. 3 operates normally when a voltage of the power source voltage supply line is higher than the normal voltage $V_{cc}/2$ to be output. In this case, the voltage of node N_2 is V_{th}, the voltage of node N_3 is $2\times V_{th}$. When $R_1=R_2$, the voltage of node N_1 is indicated by $(V_{cc}-2V_{th})/2+2V_{th}=V_{cc}/2+V_{th}$. Since the transistors Q_1, Q_3 are formed by the same process on a semiconductor substrate, these transistors can be considered to have the same threshold voltage. When the node N_1 has the above voltage, a load voltage V_{cc}' is $V_{cc}/2$, which is lower than the above voltage by V_{th}. Thereby, a voltage V_{cc}' irrespective of the threshold voltage of a transistor can be supplied to the load L.

FIG. 4 is a second embodiment of this invention. The circuit of FIG. 3 is based on the assumption that the load L always receives an input current through the transistor Q_1 (a current flows through V_{cc}–Q_1–L–V_{ss}) and that a current does not flow out from the load L toward the source of the transistor Q_1. However the circuit of FIG. 4 can operate properly even if current flows out from the load L. In this circuit, the circuit portion formed by R_1, R_2, Q_3, Q_2 is the same as that in FIG. 3, a load voltage V_{cc}' is held thereby to $V_{cc}/2$, irrespective of V_{th}. The MIS transistors Q_4, Q_5, Q_6 resistors R_3, R_4 form a circuit which holds the load voltage V_{cc}' to $V_{cc}/2$ in such a case where a current flows into the power supply V_{ss} through the transistor Q_4 from the load L. Here, Q_4, Q_5, Q_6 are P channel transistors. Namely, the voltage of node N_6 is $V_{cc}-V_{thp}$, the voltage of node N_5 is $V_{cc}-2V_{thp}$ and the voltage of node N_4 is $(V_{cc}-2V_{thp})/2=V_{cc}/2-V_{thp}$ when $R_3=R_4$. V_{thp} is the gate threshold voltage of the p channel transistor Q_4. Since a voltage of node N_4 is lower than V_{cc}' by V_{th} of Q_4, V_{cc}' becomes $V_{cc}/2$. In the circuit of FIG. 4, a load voltage can be set constant irrespective of a load voltage V_{th}, in either case where a current flows into the load or a current flows out from the load.

It is desirable in actual design of the circuit of FIG. 4 to assure the avoidance of a steady current in the series circuit of transistors Q_1 and Q_4 by providing a small difference between the voltage dividing ratio of the resistors R_1, R_2 and the voltage dividing ratio of the resistors R_3, R_4. For example, the voltage of node N_1 should advantageously be $V_{cc}/2+V_{th}$ minus several 10 mV and the voltage of node N_4 should be $V_{cc}/2-V_{thp}$ plus several 10 mV. Thereby, when the output voltage V_{cc}' is $V_{cc}/2$, both output transistors Q_1, Q_4 are set to the cut-off condition. IF the output voltage V_{cc}' rises or drops, the output transistors Q_1 or Q_4 become selectively ON and suppress the change of voltage described above.

FIG. 5 and FIG. 6 show the third and fourth embodiments of this invention. The former holds a load voltage V_{cc}' to $V_{cc}/3$, while the latter to $2V_{cc}/3$. Namely, since the voltage of node N_7 is $3V_{th}$ and the resistance values of resistors R_1, R_2 are selected in such a relation as $R_1=2R_2$ in FIG. 5, the voltage of node N_1 becomes equal to $(V_{cc}-3V_{th})/3+3V_{th}=V_{cc}/3+2V_{th}$, and the load voltage V_{cc}' is lower than this voltage level by $2V_{th}$ due to the voltage drop across transistors Q_8 and Q_1 thus becoming equal to $V_{cc}/3$. In FIG. 6, the voltage of node N_7 is $3V_{th}$, the voltage of node N_1 is $2(V_{cc}-3V_{th})/3+3V_{th}=2V_{cc}/3+V_{th}$ when $2R_1=R_2$, and the load voltage V_{cc}' is lower than this voltage by V_{th}, becoming equal to $2V_{cc}/3$.

In general, the load voltage of $V_{cc}'=mV_{cc}/n$ can be obtained by using n transistors as the transistors Q_2, Q_3, . . . to be inserted in series with the resistance voltage dividing circuit, of the gate voltage control circuit and $(n-m-1)$ transistors as the transistors Q_8 . . . to be inserted into the gate circuit of the output transistor Q_1, and by setting a resistance ratio $R_2/(R_1+R_2)$ to m/n. Thereby, a variety of load voltages V_{cc}' which are not affected by V_{th} can be obtained. In the above, m and n are integers for which $m<n$.

When the resistance value is made large in order to reduce power consumption in the resistance voltage dividing circuit, the time constant becomes large and the rising edge of the load voltage becomes gentle as shown in FIG. 7(*a*). In case a transistor Q_1 is used as in the case of FIG. 3, the load voltage V_{cc}' quickly rises as shown in FIG. 7(*b*) and, when the power supply becomes ON, operation can be started immediately.

In the circuit of FIG. 3, the resistor R_2 may be shifted, for example, to the location between Q_3 and V_{ss} from the location indicated. The alternate location for the resistor R_2 is indicated by the resistor R_2', shown with the dotted line in the lower left corner of FIG. 3. In this case, the same result can also be obtained. Moreover, this method is superior in such a point that each transistor Q_1, Q_2, or Q_3 receives a similar back gate bias effect on its own V_{th}, since the source voltage of Q_2, Q_3 rises up to a value close to that of Q_1 and, thereby, V_{th} of Q_2 and Q_3 becomes equal to that of Q_1.

FIG. 8 shows an embodiment where the resistors R_1, R_2 in FIG. 3 are replaced by depletion transistors T_1, T_n, T_1' T_n'. The same transistors and the same nodes are indicated by the same symbols. In general, a resistance of the polysilicon layer or diffusion layer used in a MIS dynamic memory is as small as several 10 ohms/square. If it is desired to obtain a resistance of several 100 k-ohm as required for the resistors R_1, R_2 by using these resistance layers, an area of several hundreds of thousand μ^2 becomes necessary. In order to avoid this, it is recommended to use one or a plurality of depletion transistors connected in series in place of resistors. Thereby, a current can be reduced using a small area.

I claim:

1. A voltage converting circuit for receiving a power source voltage and providing a constant voltage having a level of a predetermined proportional division of said power source voltage, comprising:

an output MIS transistor, having a gate and a threshold voltage, for outputting said constant voltage, wherein the gate of said output MIS transistor receives a gate control voltage; and

gate control means for providing said gate of said output MIS transistor with said gate control voltage, comprising

an output node for outputting said gate control voltage,

resistive means, including pairs of resistive elements connected in series via said output node and connected to receive said power source voltage, for determining said predetermined proportional division, each resistive element having a resistance being independent of said threshold voltage, and

compensating means, including a plurality of compensation MIS transistors connected in series with said resistive means, for compensating for the value of the threshold voltage of said output MIS transistor in the value of said gate control such that said constant voltage corresponding to said predetermined proportional division is output by said output MIS transistor irrespective of a common variation of the threshold voltage of each of said output and said compensation MIS transistors, the number of said compensation MIS transistors being in accordance with the proportion of said predetermined proportional division.

2. A voltage converting circuit as set forth in claim 1, wherein said resistive elements comprise a plurality of resistor elements connected in series with said compensation MIS transistors.

3. A voltage converting circuit as set forth in claim 1, wherein said resistive elements comprise a plurality of depletion MIS transistors connected in series with said compensation MIS transistors.

4. A voltage converting circuit as set forth in claim 1, wherein said output MIS transistor and each said compensation MIS transistor is produced in the same production process to have the same threshold voltage.

5. A voltage converting circuit as set forth in claim 1, wherein said impedance means comprises plural parts connected on opposite sides of said compensation MIS transistors.

6. A voltage converting circuit connected between first and second power source lines for supplying a power source voltage, for providing a constant voltage having an intermediate level with respect to said power source voltage, said circuit comprising:

first and second output MIS transistors respectively connected to said first and second power source lines and to each other to provide said constant voltage, the first and second output MIS transistor having respective first and second gates which receive first and second gate control voltages, respectively; and

first and second gate control means, for providing said first and second gates with said first and second gate control voltages respectively, comprising:

first and second impedance means each connected between said first and second power source lines for providing first and second proportional divisions of said power source voltage, respectively; and

first and second compensating means having first and second compensation MIS transistors connected to said first and second impedance means, respectively, for compensating the first and second gate control voltages for the respective gate threshold voltages of said first and second MIS transistors;

wherein said first and second output voltages are provided irrespective of variations of said gate threshold voltages, respectively.

7. A voltage converting circuit as set forth in claim 6, wherein each of said first output MIS transistor and said first compensation transistor comprises an N channel MIS transistor and each of said second output MIS transistors and said second compensation transistors comprises a P channel MIS transistor.

8. A voltage converting circuit as set forth in claim 6, wherein each said first and second impedance means has plural parts connected in series and on both sides of the respective first and second compensation MIS transistors.

9. A voltage coverting circuit as in claim 6, wherein at least one of said first and second output MIS transistors is in the cut-off state at any time.

10. A voltage converting circuit for receiving a power source voltage and providing a constant voltage having a level of a predetermined proporational division of said power source voltage defined by the ratio of m/n, wherein n and m are positive integers and m is less than n, comprising:

an output MIS transistor, having a gate and a threshold voltage, for outputting said constant voltage, wherein the gate of said output MIS transistor receives a gate control voltage; and

gate control means for providing the gate of said output MIS transistor with said gate control voltage, comprising

an output node for outputting said gate control voltage,

resistive means, including pairs of resistive elements connected in series via said output node and connected to receive said power source voltage, for determining said predetermined proportional division, each resistive element having a resistance being independent of said threshold voltage,

compensating means, connected in series with said resistive means, including first compensation MIS transistors, the number of said first compensation MIS transistors corresponding to the denominator n of said ratio of said predetermined proportional division,

at least a second compensation MIS transistor connected in parallel with a portion of said resistive means, for providing said gate control voltage to said gate of said output MIS transistor, the number of said second compensation MIS transistors corresponding to the numerator m of said ratio;

said gate control voltage having the level of said constant voltage plus a threshold voltage of said output MIS transistor.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 4,692,689
DATED : September 8, 1997
INVENTOR(S): TAKEMAE

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, col. 5, line 10,change "pairs" to --a pair--.

Claim 10, col. 6, line 42,change "pairs" to --a pair--.

Signed and Sealed this

Eighteenth Day of April, 2000

Attest:

Attesting Officer

Q. TODD DICKINSON

Director of Patents and Trademarks